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10/039,017	01/02/2002	David Arnold Luick	ROC920010189US1	7517

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EXAMINER	
MAI, TAN V	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,017	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Tan V Mai	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/14/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,18-29 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33* is/are allowed.

6)☒ Claim(s) *1-7,10-14,18-29,31 and 32* is/are rejected.

7)☐ Claim(s) *8,9 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant's election without traverse of Specie I, claims 1-15 and 18-29, in Paper No. filed 10/14/04 is acknowledged.

2. The abstract of the disclosure is objected to because legal phraseology is used in this paragraph (i.e., "comprise"" and "comprising"). Correction is required. See MPEP § 608.01(b).

3. Claims 21 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per independent claim 21, the phrase "generating a carry out signal from a bit location within **one** of the two binary numbers" (lines 3-4) is misdescriptive. It is noted that the "carry out signal" is the result of either a first and a second binary number or portions of a first and a second binary number. Similarly noted claim 27.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

(f) he did not himself invent the subject matter sought to be patented.

(g)(1) during the course of an interference conducted under section 135 or section 291, another inventor involved therein establishes, to the extent permitted in section 104, that before such person's invention thereof the invention was made by such other inventor and not abandoned, suppressed, or concealed, or (2) before such person's invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under this subsection, there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

5. Claims 1-7, 10-14, 18-29, 31 and 32 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Jang et al (US Pat 5,548,546).

As per independent claim 1, Jang et al teach, e.g., see Fig. 2, the claimed combination elements. The element (301) and elements (302, 303) are considered the claimed "first arithmetic logic unit (ALU)" and "second ALU", respectively.

As per dependent claim 2, the claim adds a "memory having a first memory portion receiving the first result and a second memory portion receiving the second result". Either elements (301, 302) should have memory means, such as latches, for storing the results or the results (S0-S3, S4-S7) stored in memory device.

As per dependent claim 3, the claim adds a "logic circuit for incrementing a value stored in the memory portion". Element (303) is a conditional incrementer.

As per dependent claim 4, the claim adds the "incremented value is stored in the second memory portion in response to the carry out signal". The "incremented value" (S4-S7) should be stored in the memory device in response to the carry out C1.

As per dependent claim 5, the claim adds the "second memory portion is configured to increment a value stored in the second memory portion in response to the carry out signal". The "incremented value" (S4-S7) should be stored in the memory device in response to the carry out C1.

As per dependent claim 6, the claim adds the "memory stores a value used to address a random access memory". The sum result (S0-S7) could used to address a random access memory.

As per dependent claims 7 & 10, Jang et al teach the claimed features.

Due to the similarity of claims 11-14, 18-29, 31 and 32 to claims 1-5, they are rejected under a similar rationale.

5. Claims 1-7, 10-14, 18-29, 31 and 32 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Jang et al (US Pat 5,912,833).

As per independent claim 1, Jang et al teach, e.g., see Fig. , the claimed combination elements. The element (11) and elements (12, 13) are considered the claimed "first arithmetic logic unit (ALU)" and "second ALU", respectively.

As per dependent claim 2, the claim adds a "memory having a first memory portion receiving the first result and a second memory portion receiving the second result". Either elements (11, 12) should have memory means, such as latches, for storing the results or the results (S0-S3, S4-S7) stored in memory device.

As per dependent claim 3, the claim adds a "logic circuit for incrementing a value stored in the memory portion". Element (13) is a conditional incrementer.

As per dependent claim 4, the claim adds the "incremented value is stored in the second memory portion in response to the carry out signal". The "incremented value" (S4-S7) should be stored in the memory device in response to the carry out C1.

As per dependent claim 5, the claim adds the "second memory portion is configured to increment a value stored in the second memory portion in response to the carry out signal". The "incremented value" (S4-S7) should be stored in the memory device in response to the carry out C1.

As per dependent claim 6, the claim adds the "memory stores a value used to address a random access memory". The sum result (S0-S7) could used to address a random access memory.

As per dependent claims 7 & 10, Jang et al teach the claimed features.

Due to the similarity of claims 11-14, 18-29, 31 and 32 to claims 1-5, they are rejected under a similar rationale.

7. Claims 1-7, 10-14, 18-29, 31 and 32 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Muramatsu et al (US Pat 6,832,235).

As per independent claim 1, Muramatsu et al teach, e.g., see Figs. 9 & 11, the claimed combination elements. For example, element (39 of Fig. 9) and elements (45, 38) are considered the claimed "first arithmetic logic unit (ALU)" and "second ALU", respectively.

As per dependent claim 2, the claim adds a "memory having a first memory portion receiving the first result and a second memory portion receiving the second

result". Either elements (39, 45) should have memory means, such as latches, for storing the results or the results S[14:0] & S[30:15] stored in memory device.

As per dependent claim 3, the claim adds a "logic circuit for incrementing a value stored in the memory portion". Element (38) is a conditional incrementer.

As per dependent claim 4, the claim adds the "incremented value is stored in the second memory portion in response to the carry out signal". The "incremented value" S[30:15] should be stored in the memory device in response to the carry out C14.

As per dependent claim 5, the claim adds the "second memory portion is configured to increment a value stored in the second memory portion in response to the carry out signal". The "incremented value" S[30:15] should be stored in the memory device in response to the carry out C14.

As per dependent claim 6, the claim adds the "memory stores a value used to address a random access memory". The sum result of device (37) could used to address a random access memory.

As per dependent claims 7 & 10, Muramatsu et al teach the claimed features.

Due to the similarity of claims 11-14, 18-29, 31 and 32 to claims 1-5, they are rejected under a similar rationale.

8. Claims 8-9 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cited references are art of interest.

10. The following is an examiner's statement of reasons for allowance: the recorded references do NOT teach or suggest the: "**logic circuit** selecting one of the first upper portion and the second upper portion **in response to** the first flag and the second flag bit, the selected upper portion used as the second result" as recited in dependent claims 8 and 15. Similarly language is used in independent claim 33.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (571) 272-3726. The examiner can normally be reached on Mon-Wed and Fri. from 9:30am to 2:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is:

Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Tan V. Mai
Primary Examiner